CIRCUIT AND METHOD FOR PROCESSING AN AUTOMATIC FREQUENCY CONTROL SIGNAL

This invention is related, in general, to signal conversion and, more specifically, to circuitry for signal conversion using an Automatic Frequency Control (AFC) signal.

Portable communication products require circuits that can perform well in a low power environment. A reduction of power supply voltages allows for fewer battery cells, reducing the size and weight of the portable equipment. However, the lower power constraint adversely affects the performance of the standard RF circuitry. Circuits are needed that can achieve the design goals for noise figure, linearity and power consumption for portable communications products.

In a two-way communication link, the transmit signal must be differentiated from the desired signal to be received. The received signal is passed through circuits that include low-noise amplifiers and mixers for down-converting the received signal in frequency from the Radio Frequency (RF) range to the Intermediate Frequency (IF) range. The mixer generates an output signal having a frequency that is the difference between the frequency of the received RF signal and the frequency of a local oscillator signal, thus converting the received signal to an IF signal.

The performance of filtering, frequency conversion and demodulation is sensitive to IC processing. The purpose of the receiver is to receive and process a signal while accounting for variations that affect frequency and tuning accuracy. An Automatic Frequency Control (AFC) signal is provided to adjust the receiver frequency demodulation process and accommodate operating power supply changes and component variations due to temperature and process. Typically, the AFC signal charges an external capacitor used by the tuning circuit for filtering. This capacitor value is large to prevent the oscillator from following the modulation signals and cancelling them. However, the large capacitance value limits the tuning speed of the AFC.

Accordingly, a need exists for a receiver that generates an AFC signal that has

a fast operation. It would be a competitive advantage to provide a receiver that eliminated external components.

Brief Description of the Drawings

FIG. 1 is a block diagram of an integrated demodulator that receives an Automatic Frequency Control (AFC) signal in accordance with the present invention;

FIG. 2 is a circuit diagram of one embodiment of an integrated demodulator tuning circuit;

FIG. 3 is a plot of the difference in currents supplied at the output terminals versus the current at the input terminal of the integrated demodulator tuning circuit shown in FIG. 2; and

FIG. 4 is a circuit diagram of another embodiment for an integrated demodulator tuning circuit.

Detailed Description of the Drawings

FIG. 1 is a block diagram of an integrated injection-locked demodulator circuit 2 that generates an Automatic Frequency Control (AFC) signal in accordance with the present invention. Injection-locked demodulator circuit 2 includes an injection-locked oscillator 6 and a phase detector 4, both receiving an input signal IF. It should be noted that both phase detector 4 and injection-locked oscillator 6 in circuit 3 receive the modulated signal IF. Injection-locked oscillator 6 generates an output signal to phase detector 4 that has a quadrature relationship to the received signal IF. The output signal generated by phase detector 4 is supplied to a tuning circuit 10 that generates an output signal for controlling the charge on a capacitor in low pass filter 8. The output signal from filter 8, i.e., the AFC signal, is fed back to oscillator 6 and provides control over the frequency of the oscillator. Although shown in FIG. 1 as a

single line that connects demodulator circuit 3 to tuning circuit 10, it should be understood that either a single-ended or differential signal could be provided.

In general, if the AFC made the oscillator follow low frequency modulation signals it would cancel them. To avoid this, prior art demodulators have used a very large capacitor to give a very low frequency pole in the AFC filter. In some applications, especially time division duplex systems where transceivers must switch quickly back and forth between transmit and receive, fast tuning is required and the large capacitor is not an option. In the present invention, the demodulator portion is comprised of an injection-locked oscillator 6 and a phase detector 4 that compare the phase of the oscillator to that of the injected input signal. The demodulated output signal is also filtered and used for AFC where it adjusts the oscillator frequency so that the average value of the output signal is zero.

Integrated injection-locked demodulator circuit 2 uses a small capacitor that is small enough to be integrated on a semiconductor chip. Disabling the AFC either by separating the tuning and decoding functions in time or tuning only when the oscillator is off tune allows the use of a small capacitor. Thus, when demodulator circuit 2 receives data in the modulated signal, the AFC signal generated by tuning circuit 10 is disabled. However, when data is not received in the modulated signal, the AFC signal is enabled to tune oscillator 6 to the input carrier frequency.

FIG. 2 is a circuit diagram showing one embodiment of integrated demodulator tuning circuit 10 that generates an AFC signal provided at an output terminal 48. The same reference numbers are used in the figures to denote the same elements. Demodulator tuning circuit 10 can be used for personal communications service or in a cellular phone, among others. Although P-channel MOSFETs and NPN transistors are shown in the figures, an alternate embodiment could use PNP transistors and N-channel MOSFET devices. A differential input current is received at input terminals 12 and 46 and an output current that is a function of the difference in input currents is provided at output terminal 48. The current received at input terminal 12 is mirrored in transistors 14 and 16 and again mirrored in transistors 24 and 26. Transistors 14 and

16 are P-channel devices having commonly connected gate terminals that further connect to input terminal 12. The source terminals of transistors 14 and 16 are connected to a power conductor for receiving an operating voltage V_{CC}. The drain terminal of transistor 14 is connected to input terminal 12. Transistors 24 and 26 are NPN transistors having commonly connected base terminals that further connect to the collector of transistor 24 and to the drain terminal of transistor 16. The emitter terminals of transistors 24 and 26 are connected to a power conductor for receiving an operating voltage such as ground. Thus, transistors 14 and 16, and 24 and 26 are configured to provide a current path from input terminal 12 to output terminal 48.

Transistors 36 and 40 are P-channel devices having commonly connected gate terminals that further connect to input terminal 46. The source terminals of transistors 36 and 40 are connected to the power conductor for receiving the operating voltage V_{CC}. The drain terminal of transistor 40 is connected to input terminal 46. Transistors 32 and 34 are NPN transistors having commonly connected base terminals that further connect to the collector of transistor 34 and to the drain terminal of transistor 36. The emitter terminals of transistors 32 and 34 are connected to a power conductor for receiving the ground operating voltage. Transistors 28 and 30 are P-channel devices having commonly connected gate terminals that further connect to the drain of transistor 30 and the collector of transistor 32. The source terminals of transistors 28 and 30 are connected to the power conductor for receiving the operating voltage V_{CC}. The drain terminal of transistor 28 is connected to the collector terminal of transistor 26 and to output terminal 48. Thus, current mirrors formed by transistors 40 and 36, 32 and 34, and 30 and 28 are configured to provide a current path from input terminal 46 to output terminal 48.

Demodulator tuning circuit 10 further includes a P-channel transistor 20 having a gate terminal connected to input terminal 12 and a source terminal connected to the power conductor for receiving the operating voltage V_{CC}. The drain of transistor 20 is

commonly connected to the base terminals of transistors 22 and 42 and further connected to the collector terminal of transistor 22. The emitter terminals of transistors 22 and 42 are connected to the power conductor that receives the ground operating voltage. The collector terminal of transistor 42 is connected to the drain terminal of transistor 36. A P-channel transistor 38 has a gate terminal connected to input terminal 46, a source terminal connected to the power conductor for receiving the operating voltage V_{CC} and a drain terminal connected to the collector terminal of a transistor 44. Transistors 18 and 44 are NPN transistors having commonly connected base terminals that are further connected to the collector terminal of transistor 44. The emitter terminals of transistors 18 and 44 are connected to the power conductor that receives the ground operating voltage. The collector terminal of transistor 18 is connected to the drain terminal of transistor 16. It should be noted that this embodiment of demodulator tuning circuit 10 does not include an additional input as shown in FIG. 1.

FIG. 3 is a plot of the difference in currents at input terminals 12 and 46 and the corresponding current supplied at output terminal 48 of the integrated demodulator tuning circuit 10. The x-axis represents the difference in currents supplied at input terminals 12 and 46 and the y-axis represents the current provided at output terminal 48 in response to the differential input currents. Specifically, line 70 represents the current at output terminal 48 with integrated demodulator tuning circuit 10 operating under the condition where the difference between the currents supplied at terminals 12 and 46 has a value that is above a "set threshold value", and in addition, the current supplied at input terminal 12 is greater than the value of the current supplied at input terminal 46.

Line 72 shows a dead band in the output current of integrated demodulator tuning circuit 10 operating under the condition where the difference between the currents supplied at terminals 12 and 46 is either at or below the "set threshold value". It should be noted that the mid-point on line 72 represents the condition where the

currents supplied at terminals 12 and 46 are the same, and therefore, the difference in the input currents is zero. The two end points of line 72 indicate the "set threshold value" as determined by the sizing of transistors 14, 16, 20, 36, 38 and 40. Specifically, one end point of line 72 is determined by the relative sizes of transistors 14, 16 and 20, and the other end point is determined by the relative sizes of transistors 36, 38 and 40. By way of example, transistors 20 and 38 are sized with a ratio of about sixteen and transistors 16 and 36 are sized with a ratio of about fourteen. Again, the "set threshold value" is set by design and determined by the relative geometric sizes of transistors 14, 16, 20, 36, 38 and 40 (see FIG. 2).

As mentioned, the dead band in the output current is generated by appropriately sizing selected devices in demodulator tuning circuit 10. With equal currents supplied at input terminals 12 and 46, the current sinking capabilities of transistors 18 and 42 should be greater than the current sourcing capabilities of transistors 16 and 36. As an alternate to sizing transistors 14, 16, 20, 36, 38 and 40, transistor 18 could be sized to conduct a current greater than the current conducted by transistor 44 and transistor 42 could be sized to conduct a current greater than the current conducted by transistor 22. In this embodiment the current conduction of transistors 18 and 42 would be greater than the current conduction of transistors 16 and 36.

Line 74 illustrates integrated demodulator tuning circuit 10 operating under the condition where the difference between the currents supplied at terminals 12 and 46 has a value that is above a set threshold value and the current supplied at input terminal 46 is greater than the value of the current supplied at input terminal 12.

In operation, the AFC signal supplied at output terminal 48 is used for adjusting the voltage on a filter capacitor (not shown) that controls an oscillator frequency in a demodulator. When the oscillator frequency is in tune the AFC signal can be disabled. Briefly referring to FIG. 3, the dead band, as illustrated by line 72, has been designed into integrated demodulator tuning circuit 10 for disabling the AFC signal. Now referring to FIG. 2, when the difference in currents supplied at terminals 12 and 46 has

a value less than the set threshold value, transistors 20, 22 and 42 disable the current mirror formed by transistors 32 and 34 and transistors 38, 44 and 18 disable the current mirror formed by transistors 24 and 26. The dead band in the AFC current characteristic occurs when the current mirrors are disabled. The dead band is maintained until the difference in input currents reaches a threshold value in either polarity. The dead band preserves the frequency of the oscillator and allows integration of the filter capacitor.

Another method of tuning the oscillator frequency is to provide the injection-locked demodulator with an unmodulated signal at the carrier frequency of the modulated signal. Once the oscillator is tuned, the AFC signal is disabled and the injection-locked demodulator is provided with a modulated signal to demodulate. The AFC signal is disabled in the presence of the modulated signal to prevent detuning the injection-locked demodulator.

FIG. 4 is a circuit diagram of another embodiment of an integrated demodulator tuning circuit 60. It should be noted that integrated demodulator tuning circuit 60 could be substituted for demodulator tuning circuit 10 in FIG. 2. A differential input current is received at input terminals 12 and 46 and an output current provided at output terminal 48. Similar to the configuration shown in FIG. 2, the current received at input terminal 12 is mirrored in transistors 14 and 16 and again mirrored in transistors 24 and 26. Thus, transistors 14 and 16 and transistors 24 and 26 are configured to provide a current path from input terminal 12 to output terminal 48. Also similar to the configuration shown in FIG. 2, the current received at input terminal 46 is mirrored in transistors 36 and 40, and again mirrored in transistors 32 and 34, and mirrored yet again in transistors 28 and 30. Thus, current mirrors formed by transistors 36 and 40, 32 and 34, and 28 and 30 are configured to provide a current path from input terminal 46 to output terminal 48.

In comparing the embodiments shown in FIGs. 2 and 4, transistors 18, 20, 22, 38, 42 and 44 have been removed from the embodiment shown in FIG. 4 and transistors 62 and 64, along with inverter 66, have been added. Transistor 62

functions as a switch coupled between the commonly connected base terminals of transistors 24 and 26 and the ground power conductor. Transistor 64 functions as a switch coupled between the commonly connected base terminals of transistors 32 and 34 and the ground power conductor. Inverter 66 has an input connected to input terminal 68 and an output connected to the gate terminals of transistors 62 and 64.

In operation, referring to FIG. 4, integrated demodulator tuning circuit 60 shows separate current paths for the differential input current supplied at terminals 12 and 46 to the output current supplied from terminal 48. The current path from input terminal 12 to output terminal 48 follows the current mirror formed by transistors 14 and 16 through the current mirror formed by transistors 24 and 26. The current path from input terminal 46 to output terminal 48 is through the current mirror formed by transistors 36 and 40, then the current mirror formed by transistors 32 and 34, and finally by the current mirror formed by transistors 28 and 30. The output current at the AFC pin, i.e., output terminal 48, is a function of the difference in the differential input currents supplied at input terminals 12 and 46.

The AFC output signal in integrated demodulator tuning circuit 60 is enabled by a logic high signal for the signal ENABLE that is supplied at input terminal 68. When enabled, the output voltage at terminal 48 is a function of the difference in input currents supplied at terminals 12 and 46. A logic low signal, on the other hand, disables the AFC output signal. Specifically, a logic low signal supplied at input terminal 68 causes transistor 62 to be conductive, shutting off the current mirror formed by transistors 24 and 26 and disabling the current path from input terminal 12 to output terminal 48. Further, a logic low signal supplied at input terminal 68 causes transistor 64 to also be conductive, shutting off the current mirror formed by transistors 32 and 34 and disabling the current path from input terminal 46 to output terminal 48. Thus, the logic low signal at input terminal 68 switches the AFC signal off and the output current at terminal 48 does not respond to changes in the differential input current supplied at terminals 12 and 46. The AFC signal supplied by integrated demodulator tuning circuit 60 is used for setting a voltage on a tuning capacitor in filter

88 (see FIG. 1) that controls an oscillator frequency generated in a demodulator. While the AFC signal supplied from terminal 48 is switched off, charge is held on the tuning capacitor and the frequency of the oscillator in the demodulator is preserved.

By now it should be appreciated that an integrated demodulator tuning circuit has been shown that provides a circuit and method for generating a dead band in the AFC current characteristic and, in addition, a circuit and method for switching the generated AFC signal off and on. Both the circuitry for generating the dead band and the circuitry for switching the AFC signal on/off preserve the frequency of the oscillator, allow fast tuning without interfering with the modulation, and allow integration of the filter capacitor.